MFO/M-300-a

PATENT

#8
12/7/87

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Richard A. Blanchard

Assignee: Siliconix incorporated

Title: "PLANAR VERTICAL CHANNEL DMOS STRUCTURE"

Serial No.: 06/843,454 Filing Date: 03/24/86

Examiner: T. Thomas Art Unit: 114

Attorney Docket No.: M-300 US

Santa Clara, California
October ___, 1987

COMMISSIONER OF PATENTS & TRADEMARKS
Washington, D. C. 20231

DECLARATION PURSUANT TO RULE 37 C.F.R. 1.132

Sir:

I, Dr. Richard A. Blanchard declare:

1. I am the inventor of the above U.S. Patent Application. I earned a Bachelors Degree and a Masters Degree in Electrical Engineering at Massachusetts Institute of Technology in 1970, and a Ph.D. in Electrical Engineering at Stanford University in 1982. I have been involved in the design and manufacture of transistors since 1970. Accordingly, I am an expert in the field of semiconductor technology.

2. The invention set forth in the above U.S. Patent Application provides a number of startling advantages which result in great savings of cost and silicon surface area when manufacturing transistors. In the prior art, transistor gate structures had a cross section such as illustrated in Figure 2 of the application. By constructing transistors having a cross section such as illustrated in Figure 3, it is now possible to halve the surface area of the transistor.

3. In the structure of Figure 2 of the application, it is typically necessary to leave approximately 1.5 to 2 microns

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on each side of the transistor between the source/body contact metallization and the edge of the groove. (See attached Figure A.) The grooves are typically about 2½ microns wide, the total distance from one groove to the next groove in the embodiment of Figure 2 is approximately 5.5 microns and the cell width is about 8μm.

4. By employing a structure such as the one illustrated in Figure 3, I have discovered that the transistor can be constructed while eliminating the 3 to 4 microns required on each side of the groove to allow for alignment tolerances. (See attached Figure B.) Thus, in an embodiment such as in Figure 3, each transistor cell is only 4 to 6 microns wide.

5. A typical transistor includes a large number of cells, e.g. 1000. Thus, by providing a transistor as taught in the present specification, in which the source/body regions are interdigitated with the gate, the transistor surface area can be reduced by as much as 50%, and the width of the transistor can be decreased by 4000 microns. This is a significant advantage which is extremely important when manufacturing vertical DMOS power transistors including a large number of cells.

6. Devices such as the one taught by Iwai are used in digital logic circuits and do not include a large number of cells. Therefore, any savings in surface area occurring in Iwai's structure would be quite minute compared to the reduction in surface area of the transistor of the present invention.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or

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imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Respectfully submitted,

Dated: Nov 4, 1987

Richard A. Blanchard

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner of Patents and Trademarks, Washington, D.C., 20231, November 23, 19 87.

November 23, 1987 Date of Signature

Attorney for Applicant

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